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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,476	05/17/2005	Andrea Bragagnini	007511.00003	3939
22907 7590 11/23/2010 BANNER & WITCOFF, LTD. 1100 13th STREET, N.W. SUITE 1200 WASHINGTON, DC 20005-4051				
EXAMINER				
ROCHE, JOHN B				
ART UNIT		PAPER NUMBER		
2184				
MAIL DATE		DELIVERY MODE		
11/23/2010		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Advisory Action  
Before the Filing of an Appeal Brief**

<b>Application No.</b> 10/535,476	<b>Applicant(s)</b> BRAGAGNINI ET AL.
<b>Examiner</b> JOHN B. ROCHE	<b>Art Unit</b> 2184

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 15 November 2010 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.  
Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: 1, 3-9 and 11-15.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: \_\_\_\_\_.  
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). \_\_\_\_\_  
13. ☒ Other: See Continuation Sheet

/Henry W.H. Tsai/  
Supervisory Patent Examiner, Art Unit 2184

Continuation of 13. Other:

Referring to independent claim 1, Applicant states that Leger and Walker are not suitably combined, arguing that Walker is not concerned with transferring data between two DMA controllers, but rather concerns itself with resolving issues that arise with a transfer between two modules (page 5, line 4 - page 6, line 23).

Examiner respectfully submits that in the combination between Leger and Walker, Leger teaches multiple DMA controllers, each connected to one another, and that Walker teaches, as asserted by Applicant, the transfer between two modules, "such as a processor, memory, or bus". Examiner respectfully submits that one could reasonably interpret the modules as DMA controllers, Walker's not explicitly teaching or suggesting multiple DMA controllers notwithstanding. As stated, Walker teaches connecting ports of a DMA controller to either other ports of the same DMA controller or other modules. (Walker does not appear to explicitly disqualify other DMA controllers from "other modules"). Therefore, Examiner respectfully submits that one of ordinary skill in the art at the time of invention could combine Leger with Walker to bring about coupling between two modules.

Further, Applicant states that Greene cannot be combined with Leger and Walker to bring about the claimed invention, arguing that a pipelined arrangement would not necessarily improve the throughput of the system, or even necessarily work (page 6, line 24 - page 7, line 20).

Examiner respectfully submits that the elements of each stage of the system of Greene each perform a particular step of the operation. As to Applicant's arguments that a serial connection, such as a pipelined architecture, would not necessarily provide higher throughput than a non-pipelined system (page 3, lines 10-14), Examiner respectfully submits that many high-throughput transmission buses are serial in nature, such as USB, IEEE 1394, and PCI Express.

Further, Applicant argues that "the addition of the encryption elements of Greene to the Leger/Walker system would, if anything, have the opposite effect as alleged by the Office Action" (page 7, lines 15-20).

Examiner respectfully submits that the encryption functionality of the pipelined system was not what Examiner was seeking to combine with Leger and Walker, but rather the pipelined architecture.

As to Applicant's arguments as to Examiner's motivation to combine (page 2, line 10 - page 4, line 11), Examiner respectfully submits that the connection of DMA controllers to one another was cited by Leger, while the connection of input and output buffers in particular was cited by Walker. There is nothing in Walker explicitly disqualifying other DMA controllers from being connected in such a fashion, although the modules to be connected are not explicitly described as DMA controllers. Further, as to the combination of Greene to Leger and Walker, Examiner has stated that the use of a pipelined architecture to perform functions would improve the throughput of DMA operations by splitting up the functionality between the controllers, just as each set of a combinational section and pipeline register in Greene enhances the throughput in the circuit therein.